WHAT IS CLAIMED IS:

1. A method for supporting software pipelining, comprising:

receiving a shift mask signal;

receiving a shift signal;

identifying a shifting register queue based on the shift mask signal, the shifting register queue comprising a plurality of queue registers; and

shifting the contents of the queue registers based on the shift signal.

2. The method of Claim 1, receiving the shift mask signal comprising receiving the shift mask signal from a shift mask register.

3. The method of Claim 1, receiving the shift signal comprising receiving the shift signal from an external component.

4. The method of Claim 1, the shifting register queue part of a register file, the register file comprising the plurality of queue registers and comprising a plurality of non-queue registers, the shift mask signal comprising a plurality of bits, each bit associated with a corresponding register in the register file.

5. The method of Claim 4, the bits in the shift mask signal corresponding to the queue registers comprising 1s, and the bits in the shift mask signal corresponding to the non-queue registers comprising 0s.

6. The method of Claim 4, the bits in the shift mask signal corresponding to the queue registers comprising 0s, and the bits in the shift mask signal corresponding to the non-queue registers comprising 1s.

7. A system for supporting software pipelining, comprising a register file comprising a plurality of registers, the registers comprising queue registers and non-queue registers, the queue registers forming a shifting register queue, at least one non-queue register located between two queue registers.

8. The system of Claim 7, further comprising a shift mask register operable to identify the queue registers within the register file.

9. The system of Claim 8, the shift mask register further operable to provide a shift mask signal to the register file, the shift mask signal operable to identify the queue registers for the register file.

10. The system of Claim 7, the register file further comprising write decoding logic and a plurality of multiplexers, the write decoding logic operable to generate control signals and write signals, each multiplexer corresponding to a register within the register file, each multiplexer operable to receive one of the control signals from the write decoding logic and to provide write data to the corresponding register based on the control signal.

11. The system of Claim 10, the registers within the register file comprising edge-triggered flip-flops, each register operable to receive the write data from the multiplexer and to receive one of the write signals from the write decoding logic.

12. The system of Claim 11, for each register other than a first register, the write data provided by each multiplexer to the corresponding register based on the control signal comprising data from a previous register in the register file.

13. A system for supporting software pipelining, comprising a register file comprising a plurality of registers, the register file operable to receive a shift mask signal and a shift signal, to identify a shifting register queue within the register file based on the shift mask signal, the shifting register queue comprising a plurality of queue registers, and to shift the contents of the queue registers based on the shift signal.

14. The system of Claim 13, further comprising a shift mask register operable to identify the queue registers within the register file.

15. The system of Claim 14, the shift mask register further operable to provide the shift mask signal to the register file.

16. The system of Claim 13, the shift mask signal comprising a plurality of bits, each bit associated with a corresponding register in the register file.

17. The system of Claim 13, the register file further comprising write decoding logic and a plurality of multiplexers, the write decoding logic operable to generate control signals and write signals, each multiplexer corresponding to a register within the register file, each multiplexer operable to receive one of the control signals from the write decoding logic and to provide write data to the corresponding register based on the control signal.

18. The system of Claim 17, the registers within the register file comprising edge-triggered flip-flops, each register operable to receive the write data from the multiplexer and to receive one of the write signals from the write decoding logic.

19. The system of Claim 18, for each register other than a first register, the write data provided by each multiplexer to the corresponding register based on the control signal comprising data from a previous register in the register file.

20. The system of Claim 13, the register file operable to receive the shift signal from an external component.